Please replace the paragraph beginning at page 14, line 9, with the following rewritten paragraph:

A3

--An embodiment of the present invention is shown in Fig.1, showing two OTAs (operational transconductance amplifiers) 11 and 12, in which a differential input voltage is proportional to an output current and in which a transconductance exhibits a linear characteristic. Across these OTAs, the current (K2 × gmlΔVBE) having a predetermined constant ratio K2 to an output current (gmlΔVBE) of the first OTA 11, which is proportional to a differential voltage VBE (=VBE2 – VBE1) of the base-to-emitter voltage VBE of two bipolar transistors Q1 and Q2, is caused to flow into the second OTA 12 to produce a voltage corresponding to the differential voltage ΔVBE multiplied by a constant value, that is VPTAT (= K2 × gml ΔVBE/gm2). In the second OTA 12, the base-to-emitter voltage VBE2 of the transistor Q2 is summed to VPTAT and the resulting voltage is output to produce a desired constant voltage VREF not exhibiting a temperature dependent characteristic.--

Paragraph bridging pages 16 and 17, beginning at page 16, line 21, with the following rewritten paragraph:

A4

--Such a configuration may also be used which includes a source-grounded MOS transistor MM10, having its drain and gate connected to one end and the other end of the resistor R1, respectively, a source-grounded MOS transistor MM11 having its gate connected to the drain of the MOS transistor MM10 and a current mirror circuit, having its input end connected to a drain of the MOS transistor MM11, and adapted for supplying the constant current to the MOS transistor MM10, a common source of the first and second MOS transistors

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A4. Cont.

MM1 and MM2 of the differential pair, a MOS transistor MM5 of a source follower configuration and to the collector of the bipolar transistor Q1.--

Paragraph bridging pages 17 and 18, beginning at page 17, line 7, with the following rewritten paragraph:

A5

--Referring to the drawings, certain preferred embodiments of the present invention are explained in detail. Fig.1 shows a circuit configuration of an embodiment of the present invention, as applied to a CMOS reference voltage circuit. As shown in Fig.1, this circuit includes first and second emitter-grounded transistors Q1 and Q2, each of which has a base connected to a collector and is provided with a constant current at the collector, first and second operational transconductance amplifiers (abbreviate to OTAs) 11 and 12, each of which outputs current corresponding to the voltage difference between the voltage at a positive phase(non-inverting) input terminal (+) and that at a reverse phase(inverting) input terminal (-), and a current mirror circuit 13 which has a ratio of the current input to the input end to the current output from the output end equal to a predetermined value K2. The reverse phase input terminal (-) and the positive phase input terminal (+) of the first OTA 11 are connected to the collectors(more precisely the connection nodes of the collectors and the bases) of the first and second transistors Q1 and Q2, respectively. The first OTA 11 has its output terminal connected to an input end of the current mirror circuit 13. An output end of the current mirror circuit 13 and the collector of the second transistor Q2 are connected to the positive phase input terminal (+) and the reverse phase input terminal (-) of the second OTA 12, respectively, while the output terminal of the second OTA 12 is connected to the positive phase input terminal (+) of

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A5

the second OTA 12. The reference voltage VREF is output at an output terminal of the second OTA 12.--

Please replace the paragraph beginning at page 18, line 8, with the following rewritten paragraph:

A6

--It is assumed that, in the embodiment shown in Fig.1, the emitter area of the transistor Q1 is K1 times the emitter area of the transistor Q2. The collectors of the transistors Q1 and Q2 are connected to drains of the P-channel MOS transistors M200 and M300, that is output terminals of a current mirror circuit (made up of P-channel MOS transistors M100, M200 and M300) which receives a constant current I0 from a constant current source 14 at its input terminal, and the current I0 flows through collectors of the transistors Q1 and Q2.--

Paragraph bridging pages 18 and 19, beginning at page 18, line 17, with the following rewritten paragraph:

A7

--If the DC current amplification factor of the transistors is sufficiently close to unity and the base current is neglected, from the above equation (1), the base-to-emitter voltages VBE1 and VBE2 of the transistors Q1 and Q2 are expressed as follows:

$$VBE1=VT\ln\{IC1/(K1 \cdot IS)\}$$

$$=VT\ln\{I0/(K1 \cdot IS)\} \quad (9)$$

$$VBE2=VT\ln(IC2/IS)$$

$$=VT\ln(I0/IS) \quad (10)$$--

Paragraph bridging pages 30 and 31, beginning at page 30, line 14, with the following rewritten paragraph:

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A8

--Referring to Fig.6, (K2+4) common gate P-channel MOS transistors MP1, MP2 to MP(K2+4), having respective sources connected to a power supply VDD in common, constitute a first current mirror circuit having (K2+3) outputs. The P-channel MOS transistor MP1, having its drain connected to its gate has the drain connected to a constant current source 16 with a constant current I0 being an input current to the first current mirror circuit. The drains of the P-channel MOS transistors MP2 and MP3 output a constant current to the collectors of the first and second transistors Q1 and Q2, while the drains of the P-channel MOS transistors MP4 to MP(K2+4) output a constant current to the common source of the number 1 to number K2+1 differential pairs. The transistor MN01, having its source grounded, having its drain connected to its gate, having the drain connected to the constant current source IO and fed with the sink current, and the N-channel MOS transistors MN04, MN05 and MN0(K2+3), having the sources grounded and having the gates to the gate of the transistor MN01 in common, constitute a second current mirror circuit. The transistor MN02, having its source grounded, having its drain connected to its gate, and having the drain connected to the drain of the transistor M2, and an N- channel MOS transistor MN03, having its source grounded and having its gate connected to the gate of the transistor MN02 in common, constitute a third current mirror circuit.--

Please replace the paragraph beginning at page 32, line 1, with the following rewritten paragraph:

A9

--The third to number K2 differential pairs are configured in similar manner. The diode-connected transistor M (2K2+2) of the number K2+1 last-stage differential pair has its drain connected to the drain of the output transistor MN03 of the third current mirror circuit, and is

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A9 Cont.

driven by the current proportional to that flowing in the transistor M2 of the first differential pair.--

Please replace the paragraph beginning at page 32, line 8, with the following rewritten paragraph:

A10

--The first differential pair (made up of transistors M1 and M2) is driven by the transistor MP4 with a current Io proportional to the constant current I0. If a differential voltage ΔVBE is differentially input to the first differential pair, and the drain currents flowing through the transistors M1 and M2 of the first differential pair are I1 and I2, we have

I1 + I2 = Io.

The common source of the transistors M (2K2+1) and M (2K2+2) of the last-stage number (K2+1) differential pair is fed with the current Io from the transistor MP(K2+4), the drain of the transistor M(2K2+2) is driven by the transistor MN03 with the current I2, with the current Io – I2 = I1 flowing through the drain of the transistor M(2K2+1). The differential input voltage of the number (K2+1) is ΔVBE, with the gate voltage of the transistor M(2K2+1) being lower by ΔVBE than the gate voltage of the transistor M(2K2+2).--

Paragraph bridging pages 35 and 36, beginning at page 35, line 1, with the following rewritten paragraph:

A11

--The differential pair made up of P-channel MOS transistors M1 and M2 receives a differential voltage of output voltages of the transistors Q1 and Q2. An output voltage of the transistor Q2 is applied to the gate of the P-channel MOS transistor M3 making up a second differential pair along with the diode-connected P-channel MOS transistor M4. The drain of the transistor M4 is driven with a current proportional to an output current of the first differential

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pair, that is the drain current of the transistor M2 (K3 tuple current). The common source of the first and second differential pairs is driven with two constant currents, having a certain current ratio to each other. A desired amplification factor is realized by setting the operating input voltage range of the second differential pair so as to be a preset constant number tuple of that of the first differential pair. In Fig.7, P-channel MOS transistors MP5 to MP9, which have their sources connected in common to a power supply VDD and have their gates connected in common, constitute a first current mirror circuit. The P-channel MOS transistor MP9, having its drain connected to its gate has the drain connected to a constant current source 17, with the constant current I0 being an input current to the current mirror circuit. From the drains of the P-channel MOS transistors MP5 and MP7, constant currents are fed to the collectors of the first and second transistors Q1 and Q2, and from the drains of the P-channel MOS transistors MP6 and MP8, constant currents are fed to the commonly connected sources of the first and second differential pairs respectively. An N-channel MOS transistor MN10, having a source grounded, having a drain and a gate connected to each other and having the drain connected to the drain of the transistor M2, and an N-channel MOS transistor MN11, having a source grounded and having a gate connected to the gate of the transistor MN10, constitute a second current mirror circuit.--

All Cont.

Please replace the paragraph beginning at page 37, line 1, with the following rewritten paragraph:

--The sources of the transistors M1 and M2 are connected to the drain of the P-channel MOS transistor MP6, forming an output of the first current mirror circuit. From the conditions for the driving current,

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A12

$I_{D1} + I_{D2} = I_0$ (23)--

Paragraph bridging pages 41 and 42, beginning at page 41, line 7, with the following rewritten paragraph:

A13

--In Fig.8, transistors MM1 to MM7 constitute a voltage follower type operational amplifier with a resistance for compensation RC and a capacity for compensation CC. The W/L ratio of input differential transistors MM1 and MM2 is set to 1:K2, and the W/L ratio of active load transistors MM3, and MM4, operating as loads, is set to K3:1, so that input offset is produced. The transistors MM1 and MM2, having sources connected in common to a drain of the constant current source transistor MM6, form a differential pair. The transistor MM3, connected to the drain of transistor MM1, and having its source grounded, and the transistor MM4, having its drain connected to the drain of the transistor MM2, having its source grounded and having its gate connected to the gate of the transistor MM3, form a current mirror circuit operating as a load for the differential pair. The drain of the transistor MM2, forming an output of the differential pair, is connected to the gate of the transistor M5, the drain of which is connected to a drain of the constant current source transistor MM7. An output voltage VREF is taken at a drain of the transistor MM5, operating as an output terminal. The output terminal is connected to the gate of the transistor MM2 that operates as an inverting input terminal of the differential pair. A resistor RC for phase compensation and a capacity CC are connected across the drain and the gate of the transistor MM5. A base-to-emitter voltage VBE of the transistor Q1 is input to a non-inverting input terminal of the differential pair.--

Please replace the paragraph beginning at page 42, line 10, with the following rewritten paragraph:

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A14

--The drain currents ID1 and ID2 of the respective transistors MM1 and MM2 are given by:

$$I_{D1}=\beta(V_{GS1}-V_{TH})^2 \quad (33)$$

$$I_{D2}=K3\beta(V_{GS2}-V_{TH})^2 \quad (34)$$

The following relationship holds:

$$I_{D1}+I_{D2}=I_0 \quad (35)\text{--}$$

Please replace the paragraph beginning at page 42, line 20, with the following rewritten paragraph:

A15

--Moreover, from the conditions of the active load transistors MM3 and MM4, we have

$$K3I_{D1}=I_{D2} \quad (37)$$

Solving the equations (35) and (37),

$$I_{D1}=I_0 K3/(K3+1) \quad (38)$$

$$I_{D2}=I_0/(K3+1) \quad (39).\text{--}$$

Please replace the paragraph beginning at page 44, line 5, with the following rewritten paragraph:

A16

--A circuit comprised of a transistor MM10, having a source grounded, a drain connected to one end of a resistor R1 and having a gate connected to the opposite end of the resistor R1, a transistor MM11, having a source grounded and having a gate connected to the drain of the transistor MM10, and the resistor R1, makes up a Nagata current mirror circuit. Here, with the transistors MM13 and MM12 forming a current source, the transistors MM10 and MM11 and the resistor R1 form a self-biased Nagata current mirror circuit.--

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Please replace the paragraph beginning at page 44, line 14, with the following rewritten paragraph:

A17

--Here, the transistor MM10 is assumed to be a unit transistor, and the ratio of the gate width W to gate length L, or (W/L), of the transistor MM11, is assumed to be K1 times that of the unit transistor, where K1 > 1.--

[Please replace the paragraph beginning at page 44, line 18, with the following rewritten paragraph:]

--In the MOS Nagata current mirror circuit, shown in Fig.8, the device is assumed to exhibit satisfactory matching, the channel length modulation and the substrate effect are neglected, and the relationship between the drain current and the gate-to-source voltage of the MOS transistor is assumed to follow the square rule. Then, the drain current ID1 of the MOS transistor MM10 is given by:

$$I_{D1}=\beta(V_{GS10}-V_{TH})^2 \qquad (42).--$$

Please replace the paragraph beginning at page 45, line 1, with the following rewritten paragraph:

A18

--The drain current ID2 of the MOS transistor MM11 is given by:

$$I_{D2}=K1\beta(V_{GS11}-V_{TH})^2 \qquad (43)$$

There is also the following relationship:

$$V_{GS10}=V_{GS11}+R1I_{D10} \qquad (44).--$$

Please replace the paragraph beginning at page 46, line 2, with the following rewritten paragraph:

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A19 TH

--It is noted that transistors MM11 and MM10 make up a current mirror circuit, while the transistors MM13 and ~~MM14~~ MM12 drive MM10 and MM11, respectively. Thus, the transistors MM11 and MM10 make up a MOS self-biased Nagata reference current circuit, with

$$I_{D10}=I_{D11} \quad (46)$$

Thus,

$$\Delta V_{GS}=V_{GS10}-V_{GS11}=R_1 I_{D10} \quad (47)$$

Solving the equation (39) from the equation (37),

[0149]

$$I_{D10}=I_{D11}=\frac{1}{R_1^2\beta}\left(1-\frac{1}{\sqrt{K_1}}\right)^2 \quad (48)$$ --

Please replace the paragraph beginning at page 47, line 7, with the following rewritten paragraph:

A20

--Also, the transistor MM12 forms a current mirror circuit with the transistor MM13, so that

$$I_{D12}=I_{D13} \quad (51).$$--

Please replace the paragraph beginning at page 50, line 8, with the following rewritten paragraph:

A21

--Since the circuit of the present embodiment takes the configuration of a voltage follower type operational amplifier, it is possible to subtract the offset voltage. In this case, the connection of various circuit components may be kept unchanged as shown in Fig.8 and only the gate W/L ratio of the transistors MM1 and MM2 and the gate W/L ratio of the transistors

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A21 Cont.

MM3 and MM4 are changed to K2:1 and to 1:K3, respectively. The output voltage VREF of the reference voltage circuit in this case is given by:

VREF=VBE1-VOS (57).--

Please replace the paragraph beginning at page 51, line 2, with the following rewritten paragraph:

A22

--Fig.9 shows a modification of the embodiment shown in Fig.8. The drain and the gate of the transistor MM2 of the differential pair are connected together and the output VREF is taken out from the drain. In Fig.9, the output voltage VREF of the reference voltage circuit is given by:

VREF=VBE+V_{OS},

as in equation (54), where V_{OS} is given by the equation (53).

That is, a reference voltage not dependent upon temperature is output, as mentioned above. Although this modification lacks in capability of feeding a current from the reference voltage output terminal, it is effective as a voltage source for supplying the reference voltage.--

Please replace the paragraph beginning at page 52, line 10, with the following rewritten paragraph:

A23

--The reason is that, in the reference voltage circuit of the present invention, the circuitry is constructed merely using active devices, without employing resistors as in the conventional circuitry shown in Fig.10.--

IN THE CLAIMS:

Please amend claims 2-11, 17-21 and 27, to read as follows:

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